ISSN: 0974-8571 Vol.13 No. 2 December, 2021

International Journal of Computational Intelligence in Control

Enhancing Power Quality Making Use of a Multi-Level Inverter with Fewer Switching Devices and Lowest Standing Voltage.

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ABSTRACT

Photovoltaic (PV) systems' power quality has been significantly improved by the widespread use of multilevel inverters (MLIs). However, the efficiency of a standard MLI is significantly impacted by the requirement for a large number of components, increased standing voltage, and high harmonic content in the output. Therefore, asymmetrical MLIs have been created as a good substitute to deal with these problems. The goal of the current study is to create a hybrid asymmetrical structure with a high level per component ratio and a low standing voltage that is appropriate for PV applications. An RSHB MLI structure with ansymmetrical repeating units and various level doubling circuit (LDC) combinations is used to assemble the suggested MLI. The suggested MLI structures, i.e., PS1 and PS2, may synthesis 4n+5 and 4n+7 levels, respectively, at the output instead of 2n+3 levels with merely RSHB MLI since the two dc sources employed in the repeating units have a voltage ratio of 1:n. According to a comparison, PS1 and PS2 both have fewer switches, a low standing voltage, reduced power loss, and are less expensive. For the purpose of evaluating the PS1 structure's performance, a 3.9 kW standalone solar PV system is taken into account. Both the selective harmonic elimination (SHE) and carrier-based pulse width modulation (PWM) control techniques are used. This justifies the LDC's self-voltage balancing mechanism and dc-link voltage balancing.

INTRODUCTION

Multilevel inverters (MLIs) have been evolved as an emerging power electronics converter in recent years. MLIs can produce high-quality output with lower switching frequency operation, thereby reducing the voltage stress, harmonic in the output, electromagnetic interference, switching loss, etc., compared to conventional two-level inverters in the process of electrical energy conversion. Due to their competency in solving the above issues, research focus has attracted MLI for numerous applications such as electric drives, electric vehicles, railways, aircraft, and renewable energy systems. By the proper arrangement of dc-link, semiconductor switches, diodes, and capacitors, MLI produces a staircase output. MLIs are broadly classified into three categories, such as single dc-source flying capacitor MLI (FC MLI), single dc-source diode clamped MLI (DC MLI), multiple dc-sources cascaded H-bridge MLI (CHB MLI)

Regarding voltage balancing, design complexity, size, and cost [5], [10], the CHB MLI has a number of benefits. Because of this, CHB topology is mostly taken into account by researchers for progress and is suited for a variety of low voltage (230 V) to high voltage (>10 kV) level applications. The primary worry among researchers is the reduction in the number of semiconductor switches in MLI. In this regard, a number of MLI topologies that address the aforementioned problems have recently been designed. There has been an effort to lower the device counts. These topologies require approximately half as many switches as a typical CHB MLI does. However, higher voltage limits the switches' ability to operate due to increased voltage stress.

While this is going on, a few optimised MLI structures that were designed in can synthesise many levels at the output with fewer switches. These topologies, in contrast to the CHB MLI, can naturally produce negative levels. Voltage stress is a crucial factor that must be taken into consideration while planning the MLI for certain applications. In response to the aforementioned issue, the authors in have presented novel MLI topologies with a strategy to decrease both the voltage stress and the device count. A well-known method to produce many levels at the output is to use dc sources of the proper magnitude. Examples of this approach in use are topologies. For the purpose of determining the dc source magnitude, the authors have created a number of algorithms.

The choice of appropriate algorithms is a crucial element that will lead to the development of the highest levels feasible with little voltage stress on the switches. In addition to the widespread use and popularity of H-bridge based MLIs, one of the active research areas is the construction of various hybrid MLI structures. For instance, the MLI packed U cell compact module type MLI in [21] generates multilevel output without the need for an H-bridge. These modules/basic units can be cascaded in this situation to increase the number of tiers. On the other hand, the development of the level doubling circuit (LDC) has significantly advanced MLI technology.

LDCs integrated with MLI at different voltage magnitudes can be utilised to double the number of levels at the same active switch count. Recent years have seen the development of various pulse width modulation (PWM) methods as a primary concern for managing the voltage and current quality by producing the proper switching pulse for MLI. PWM control approaches are broadly divided into two classes, such as fundamental/low switching frequency control technique and high switching frequency control technique, depending on the operating frequency.

Techniques for high switching frequency control that use carrier-based PWM are highly effective in reducing THD levels and current waveform distortions. The only issue with these methods is increased switching loss. On the other hand, switching loss can be considerably decreased employing low switching frequency management approaches. One of the main switching control strategies that is frequently used to entirely attenuate the intended lower order harmonics is selective harmonic elimination (SHE). To find the best switching angles in this regard, a few rigorous mathematical calculations-based methodologies have been devised.

Additionally, popular stochastic techniques based on optimization algorithms like the genetic algorithm (GA), colonial competitive algorithm, cuckoo search algorithm (CSA), particle swarm optimization (PSO), etc., are examined critically with respect to equal and unequal dc sources. When MLIs are integrated with renewable sources, another method for optimal harmonic mitigation, i.e., to reduce each of the undesired harmonics along with calculation of appropriate switching angles, has been investigated. Further discussion thoroughly examines the suitability of photovoltaic (PV) system integration with the framework suggested in this work. In this situation, critical evaluation is required of concerns such as decreased power transfer level, MPPT failure, voltage balancing of dc-link, etc.

Literature survey

Enhancing Power Quality of Modified Multilevel Inverter with Fewest Switches

It Presents a modified nine level inverter design and execution for enhancing power quality with fewer switches. Here, we concentrate on two techniques: the modified inverter topology and the cascaded H Bridge multilevel inverter topology. Both approaches make use of a pulse generator to create the proper switching pulses. When compared to a cascaded H-Bridge multilevel inverter, the improved topology's output quality is superior. When the levels are raised in the redesigned topology, fewer switches are needed than with a cascaded H bridge inverter. As a result, it lowers upfront costs and circuit complexity, making it suitable for industrial applications. The operation of the redesigned topology is described, and MATLAB/SIMULINK software is then used to assess the outcomes.

An analysis of multilevel inverters with fewer Switches

Multilevel inverters have sparked a new wave of interest in business and research. While established topologies have become a viable option in a wide range of high-power, medium-voltage applications, there has been a strong drive for the development of newer topologies. A key goal of the recently described topologies has been to reduce overall part considerations in comparison to the traditional topologies. This research studies and evaluates a subset of the starting late proposed multilevel inverter topologies with fewer power switches. This essay will act as a companion and a redesign for these topologies, in terms of both arbitrary and objective criteria.

Topologies, Comprehensive Analysis, and Comparative Evaluation of a Recently Developed Reduced Switch Multilevel Inverter for Renewable Energy Integration and Drives Application

As they develop into a practical technology for many applications, including drives and systems for converting renewable energy, multilevel inverters (MLIs) have attracted a lot of attention from both industry and academics. One of the most cutting-edge power converter topologies, MLIs are frequently employed for these high power and high/medium voltage applications. Current research has focused heavily on the creation of reduced switch MLI (RS MLI) topologies, which can deliver high-quality output without the use of many switches. As a result, the focus of this review paper is on many recently created MLIs employed in various applications.

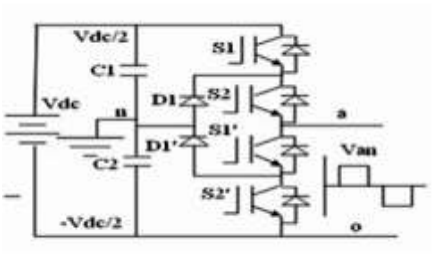
To assist with advanced current research in this field and in the selection of suitable inverter for various applications, significant understanding on these topologies is clearly summarized based on the three categories, i.e., symmetrical, asymmetrical, and modified topologies. This review paper also includes a comparison based on important performance parameters, detailed technical challenges, current focus, and future development trends. By a suitable combination of switches, the MLI produces a staircase output with low harmonic distortion. For a better understanding of the working principle, a single-phase RS MLI topology is experimentally illustrated for different level generation using both fundamental and high switching frequency techniques which will help

the readers to gain the utmost knowledge for advance research.

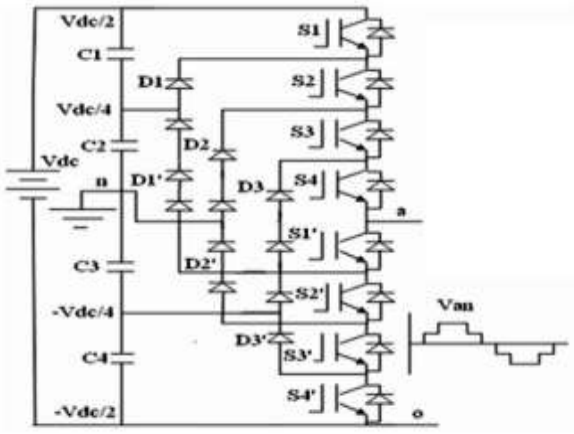
Proposed Methodology

Diode Clamped multilevel inverter

The diode clamped inverter, in which the diode is utilised as the clamping device to clamp the dc bus voltages so as to achieve steps in the output voltage, is the most widely used multilevel structure. The fundamental idea behind this inverter is to use diodes to reduce the voltage stress on the power devices. Each capacitor and switch is exposed to a voltage of Vdc. Two (n-1) switching devices, (n-1) (n-2) diodes, and (n-1) (n-1) voltage sources are required for a n level inverter. 5 level multilevel inverter with clamped diodes. Two pairs of switches and two diodes make up a three-level diode clamped inverter. Each switch pair operates in complementary mode, and access to the mid-point voltage is provided by the diodes. In inverters with three levels A commond cbus that has been subdivided into three levels by two capacitors is shared by all three of the inverter's phases. The DC capacitors C1 and C2 are connected in two series connections to divide the DC bus voltage into three voltage levels. voltage pressure



(a)



(b)

switchingdeviceislimitedtoVdcthroughtheclampingdiodesDc1andDc2. Given that the midpoint is controlled at half of the DC link voltage and that the overall DC link voltage is Vdc, the voltage across each capacitor is Vdc/2 (Vc1=Vc2=Vdc/2). Three alternative switching modes that apply the stair case voltage on the output voltage in relation to the DC link capacitor voltage rate are conceivable in a three level diode clamped inverter. A set of two switches are always active in a three-level inverter, while four switches are always active in a five-level inverter.

A phase-leg a voltage and a phase-leg b voltage make up the line voltage Vab. For a three-level inverter, the resulting line voltage has a 5-level staircase waveform and a 9-level staircase waveform for a five-level inverter. So an N-level diode clamped inverter has a (2N-1) level output line voltage in addition to a N level output phase voltage. The voltage across each capacitor for an N-level diode clamped inverter is typically Vdc/ (N-1). The clamping diodes need distinct ratings for reverse voltageblocking even if each active switching device is only required to block a voltage level of Vdc.

a three-level diode-clamped converter with two capacitors, C1 and C2, acting as the dc bus. The voltage across each capacitor is Vdc/2, the fordc-bus voltage is Vdc, and the clamping diodes will limit the voltage stress on each device to one capacitor voltage level Vdc/2. Neutral point is taken into consideration as the output phase voltage reference point to illustrate how the staircase voltage is synthesised. To create three-level voltages across a and n, there are three switch combinations.

1.Voltage level Van= Vdc/2, turn on the switches S1 andS2.

2. Voltage level Van= 0, turn on the switches S2 and S1′.

3. Voltage level Van= -Vdc/2 turn on the switches S1′,S2′.

a five-level diode-clamped converter with four capacitors (C1, C2, C3, and C4) making up the dc bus The voltage across each capacitor for dc-bus voltage Vdc is Vdc/4, and clamping diodes will limit each device's voltage stress to one capacitor voltage level of Vdc/4.

There are five switch combinations to synthesize five level voltages across a and n.

1) Voltage level Van= Vdc; turn on all upper switches S1, S2, S3 andS4.

2) Voltage level Van= Vdc/2, turn on the switches S2, S3, S4 andS1′.

3) Voltage level Van= 0, turn on the switches S3, S4, S1′ andS2′.

4) Voltage level Van= -Vdc/2 turn on the switches S4, S1′, S2′,S3′.

5) Voltage level Van= -Vdc; turn on all lower switches S1′, S2′, S3′ andS4′.

Flying Capacitor MultilevelInverter

This inverter's structure is comparable to that of a diode-clamped inverter, with the exception that capacitors are used in their place of clamping diodes. Switching cells with capacitor clamps are connected in series to create a flying capacitor. The voltage on each capacitor in this architecture is different from the voltage on the capacitor behind it, forming a ladder structure of dc side capacitors. The size of the voltage steps in the output waveform is determined by the voltage increment between two adjacent capacitor legs.

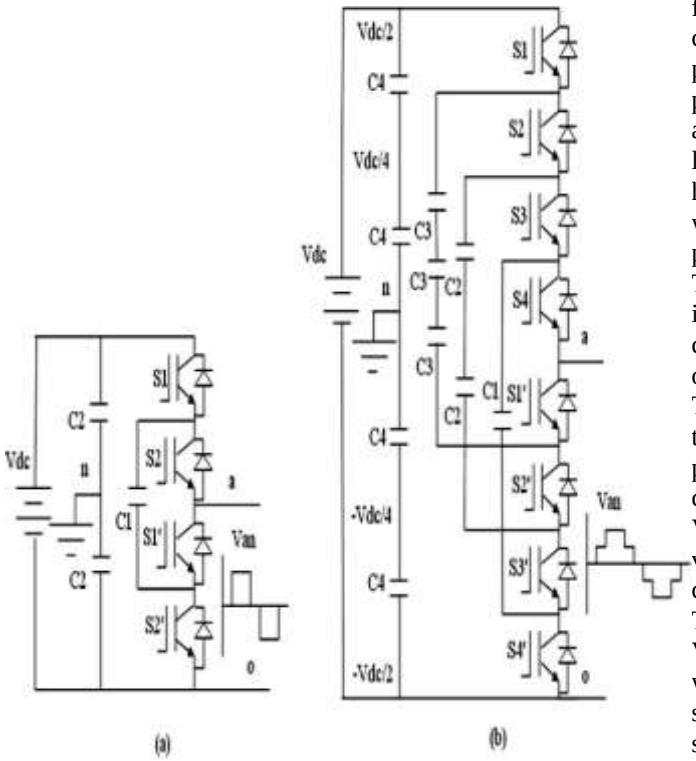


Fig 2.2 Capacitor-Clamped multilevel inverter circuit topologies (a) 3-level inverter (b) 5-level inverter

Operation of FCMLI

Each phase node (a, b, or c) in the operating capacitor multi-level inverter can be connected to any node in the capacitor bank (V3, V2, V1). When S1 and S2 are turned on, the a-phase is connected to the positive node V3; when S2 and S1′ are turned on, the a-phase is connected to the voltage at the neutral point. When both S1′ and S2′ are turned on, the negative node V1 is linked. When S1 and S1′ are turned on, the clamped capacitor C1 is discharged. The same thing happens when S2 and S2′ are turned on. Correct selection of the zero states can balance the capacitor's charge. In comparison to the three-level diode-clamped An additional switching state is achievable in an inverter. The level V3 is composed of two transistor states specifically. By choosing to charge or discharge the capacitor based on the direction of the a-phase flying capacitor current Ia for the redundant states, the capacitor voltage can be controlled to the desired value by switching within the phase. The highest and lowest switching states, similar to the three-level flying capacitor inverter, have no effect on how charged the capacitors are. Both capacitors can be controlled to their optimal voltages using the redundant states present at the two intermediate voltage levels.

Cascaded Multilevel Inverter

The CMI creates its output by merging numerous separate voltage levels into approximately sinusoidal voltage waveforms. It is possible to achieve built-in redundancy against individual Hbridge converter failure by only increasing the number of H-bridge converters without redesigning the power stage. A phase for the inverter is made up of a string of single-phase complete bridges. A three-phase CMI architecture primarily consists of three identical phase legs of a series-chain of H-bridge converters, which has the ability to produce various output voltage waveforms and provides the possibility of AC system phase-balancing.

The series connection of single-phase inverters with independent dc sources is the foundation of the converter topology. the power circuit for one phase leg of a cascaded inverter with three, five, or seven levels. The voltages generated by the various cells are added to create the phase voltage that results. Each single-phase full-bridge inverter in a 3-level cascade inverter creates three voltages at the output: +Vdc, 0Vdc, and -Vdc (zero, positive dc voltage, and negative dc voltage). The power switches are used to successively connect the capacitors to the ac side in order to do this. The output ac voltage that results fluctuates between -Vdc and +Vdc with three levels, -2Vdc and +2Vdc with a five-level inverter, and 3Vdc and +3Vdc with a seven-level inverter. Even without filtering, the staircase waveform is essentially

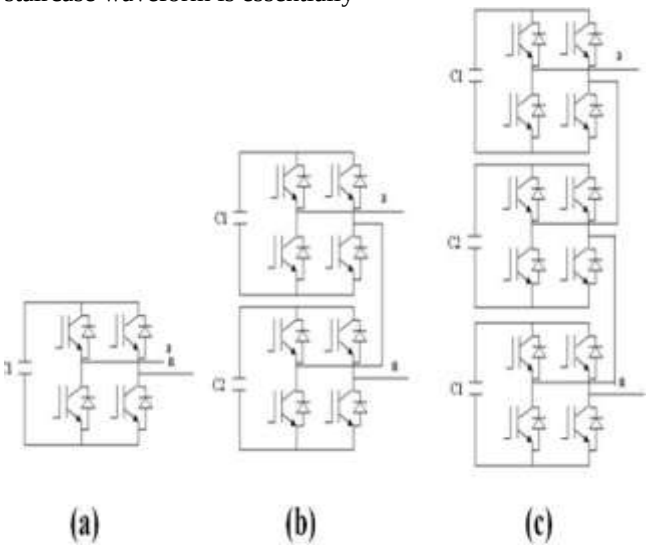


Fig2.3 Single phase structures of Cascaded inverter (a) 3-level, (b) 5-level, (c) 7-level

Cascaded H - bridge multilevelinverter

The cascaded H-bride multi level inverter uses switches and capacitors and needs fewer components

per level. Power may be easily scaled with this design, which consists of a succession of
power conversin cells. An H-bridge is a pair of

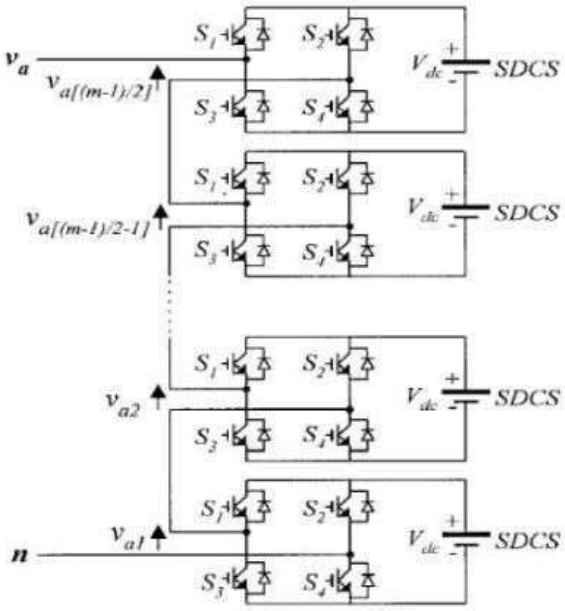


Fig2.4 Single phase structure of a cascaded H-bridge inverter

capacitors and switches that provides a distinct input DC voltage for each H-bridge. It is made up of H-bridge cells, each of which may supply one of three different voltages (zero, positive DC, and negative DC). When compared to diode clamped and flying capacitor inverters, this form of multi level inverter has the advantage of requiring fewer components. The inverter is less expensive and heavier than the other two inverters.

The idea behind this inverter is to provide a sinusoidal voltage output by series-connecting H-bridge inverters. The total voltage produced by all of the cells makes up the output voltage. There are 2n+1 levels of output voltage, where n is the number of cells. It is possible to select the switching angles to minimise total harmonic distortion. This type of multilevel inverter has the advantage of requiring less components than flying capacitor or diode clamped inverters, which lowers the cost and weight of the inverter in comparison to the two earlier types. This inverter uses the same method for calculating switching angles.

5 - level Cascaded H - bridge multilevel inverter

Similar to earlier multilevel inverters, this one provides a 5-level output voltage. This inverter is made up of two cascaded H-bridge inverters. Eight switching devices are required for a cascaded H-bridge multilevel inverter with five levels. Multilevel inverter with 9 levels cascaded over a H bridge.

9 - level cascaded H - bridge multilevel inverter

Similar to earlier multilevel inverters, the output voltage of this one has nine levels. This inverter is made up of four cascaded H-bridge inverters. There are 16 switching devices required for an H-bridge multilevel inverter with 9 levels.

11 - level Cascaded H - bridge multilevel inverter

A chain of H-bridge (single-phase full bridge) inverter units makes up a cascade multilevel inverter. Every H-bridge component has a separate dc source. Each single-phase full-bridge inverter is connected to a separate DC source (SDC). Different level inverters' ac terminal voltages are connected in series. a cascaded H-bridge inverter with distinct DC sources in a single-phase arrangement. Each converter level can produce one of three different voltage outputs—plus, minus, or zero—by combining the four switches, S1 through S4. Switches S1 and S4 are turned on to obtain +Vdcswitches. We receive the output-Vdc when S2 and S3 are turned on simultaneously. When the switches S1, S2, S3, and S4 are turned on simultaneously, we receive the output 0.

Different fullbridge converters' AC outputs are connected in series such that the synthesised voltage waveform is the sum of the outputs from each converter. The number of output-phase voltage levels in this architecture is determined by M=2N+1, where M is the number of levels and N is the number of DC sources. So, as an example, Van=Va1+Va2+Va3+Va4+Va5 gives the output phase voltage of an even level inverter.

NEUTRAL POINT-CLAMPED MULTILEVEL INVERTER

Two series-connected capacitors, C1 and C2, make up the three-level Neutral Point-Clamped inverter. The DC-link capacitors divide the DC bus voltage into three levels. These voltage levels are produced at the inverter's output of each phase by the power semiconductor devices being switched in the proper manner. The neutral point, or "n," is the centre point of the two capacitors. In this inverter, each phase contains two clamping

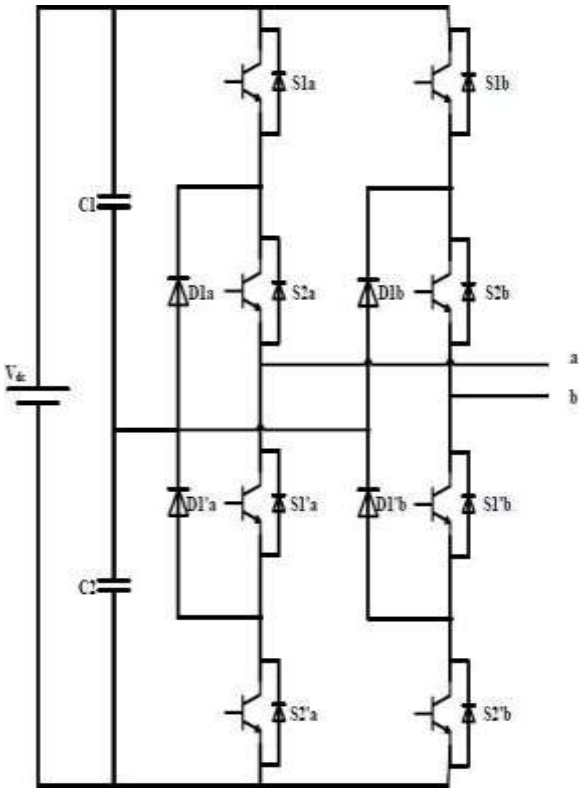


Fig2.5 Neutral point-clamped multilevel inverter

diodes (D1, D1'), two complementary switch pairs (S1, S1'), and two complementary switch pairs (S2, S2'). While the inner two switches are the auxiliary switching devices (S2,S1') that clamp the output terminal potential to the neutral point potential with the aid of the two clamping diodes, the outer two switches are the primary switching devices (S1, S2') that function for pulse width modulation.

The voltage across "a" (the first phase) and "0" (the negative inverter terminal), commonly known as the pole voltage, is Vdc when both of the upper switches S1 and S2 are turned on. The voltage sharing between the two lower diodes is balanced by the lower clamping diode, D1'.

S1' and S2' are switches. Similarly to how switch S1' blocks the voltage across C1, switch S2' does the same for C2. In contrast to the voltage between "a" and "n," which is an AC voltage, the voltage between "a" and "0" is a DC voltage. This is because the voltage across each capacitor is represented by the voltage appearing with respect to the negative inverter terminal ('0'), and the voltage appearing with respect to the inverter's neutral point ('n') is the sum of the capacitor voltages.

In order to obtain three levels across 'a'and'n', there are three switch combinations as follows:

- Turn on upper switches, S1 and S2, in order to obtain Van=+V*dc/2*.
- Turn on middle switches, S2 and S1', in order to obtain Van =0.
- Turn on lower switches, S1' and S2', in order to obtain Van=-V*dc/2*.

If we assume that each blocking diode has the same voltage rating as the active device and that each power device must block a voltage level of (Vdc/m-1) then the number of diodes needed for each phase will be (m-1) x (m-2). The relationship between the number of diodes and the level count of the multilayer inverter is quadratic.

Conclusion

In this paper, an asymmetrical DC source-based multilevel inverter is suggested. The proposal uses the fewest switches, and a voltage waveform with 17 levels is produced. The fundamental benefit of this inverter topology is that, in the asymmetric mode of operation, it only requires one DC supply and nine main switches to produce an output voltage with a 17-level distribution. When compared to earlier topologies, the overall THD (Total Harmonic Distortion) is relatively low, which improves the quality of the output waveform. The use of fewer switches allows for better circuit layout and packaging, which lowers the cost of building the suggested inverter. When comparing the two topologies, it is discovered that the proposed topology is more

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