

# Switched Capacitor Inverter Topology Photovoltaic Applications

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## ABSTRACT:

This research proposes a novel switching capacitor inverter topology for solar applications. The inverter can convert low voltage direct current (DC) into high voltage DC and then, in a single stage, invert it to the necessary voltage level with excellent quality. Comparing the suggested inverter to the traditional multilevel inverter topology, the proposed inverter features a distinctive extended structure that minimises the number of parts and devices. Additionally, some of the switches in the architecture work at low frequencies, which reduces switching losses and boosts efficiency. By using level-shifting carrier-based Pulse Width Modulation (PWM) technology, which keeps the capacitor voltages balanced, the inverter is switched. The results of a simulation conducted in MATLAB/SIMULINK to validate the suggested topology operation are presented. The proposed inverter is thoroughly compared to other inverters that have been suggested in the literature.

## KEY WORDS:

Switched Capacitor, Multilevel inverter, Voltage balancing in capacitors, Level shifted PWM technique.

## INTRODUCTION

Multilevel inverters (MLIs) have recently gained popularity among researchers who study topics like renewable energy integration and high power converters, among others. MLIs can produce waveforms that are almost sinusoidal, which helps with the power quality issue. In essence, MLIs convert a number of DC voltage sources into a high-quality AC voltage waveform. Cascaded H bridge inverter topology, diode clamped inverter topology, and capacitor clamped inverter topology are the three general types into which MLIs fall.

The main disadvantage of diode clamped inverter topology is that it shares unequal voltage between series connected capacitors and also it requires many diodes to produce more number of voltage levels at the output. Some of the advanced diode clamped inverter topologies are presented in [1]-[4]. In those topologies, active devices take the place of diodes, but because of the high total conduction voltage at zero vectors, conduction losses are increased. Numerous H bridges are connected in series to form a cascaded MLI. A distinct DC supply is necessary for each H Bridge. When all of the H Bridge's DC sources have the same magnitude, the configuration is said to be symmetrical; however, if the magnitudes of the DC sources differ, the design is said to be asymmetrical. Asymmetrical arrangements can provide more numbers when compared to a symmetrical design, levels at the load. When compared to symmetrical configuration, regulating the asymmetrical configuration is significantly more difficult. Additionally, for higher levels in both configurations, there are more DC sources and devices.

Photovoltaic (PV) applications, generally requires a DC-DC boost converter to step up a low DC voltage into a high DC voltage as required by the grid or the standalone load. This high DC voltage is again inverted into AC voltage using a high quality MLI. Thus it requires two stages of conversion. First stage is to step up the low voltage DC of PV into high voltage and the second stage is to convert the high DC voltage generated from first stage into AC voltage of high quality. Thus this two stage conversion increases the system complexity and reduces the efficiency of the system. This paper proposes a new extendable capacitor clamped MLI using switched capacitor topology. Further the proposed inverter uses a level shifting carrier based Pulse Width Modulation method to trigger the devices of the inverter. The main advantage of the proposed inverter is that the number of components used is minimized due to its combined structure. Further the proposed inverter can be extended to any required number of levels just by adding four switches and four capacitors. The remaining part of the paper is organized as follows. Topology derivation is derived in section II. In section III PWM topology for capacitor voltage balancing is dealt in detail. Finally, simulation results are detailed in Section III.

**PROPOSED TOPOLOGY**

The proposed topology is shown in figure 1, which consists of conventional H bridge and a switched capacitor network connected to the front end of the conventional H bridge. The switched capacitor topology (SCT) is proposed in [5]-[8] as shown in figure 1 in dotted structure. The SCT has four capacitors and eight power devices. Switches  $S_1, S_4, S_{1B}, S_{2A}$  are named as  $S_P$  switches and  $S_2, S_3, S_{1A}, S_{2B}$  are named as  $S_N$  switches. The operation of the proposed inverter has two states. In state A  $S_P$  switches are turned ON and in state B  $S_N$  switches are turned ON as shown in figure 2(a) and 2(b) respectively.

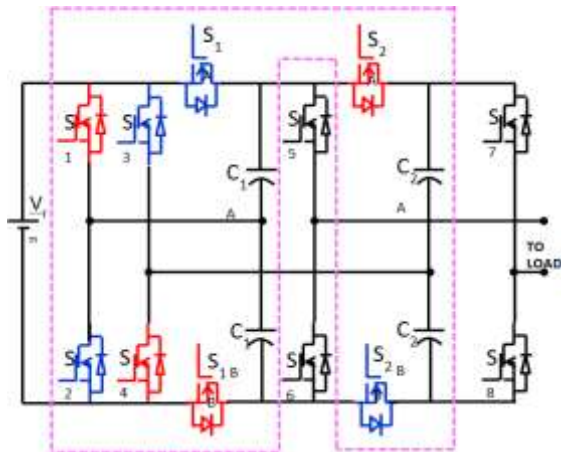


Fig 1. Proposed Inverter

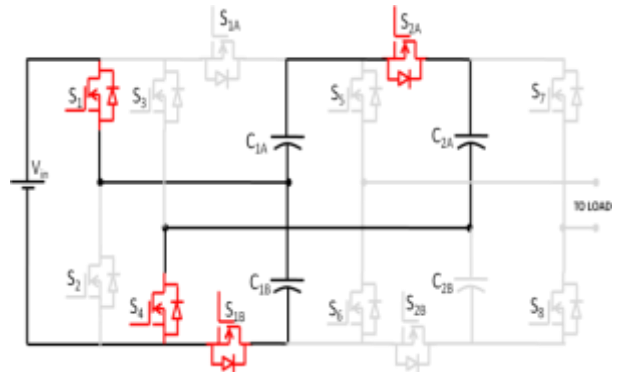


Fig 2(a)

Fig 2(b)

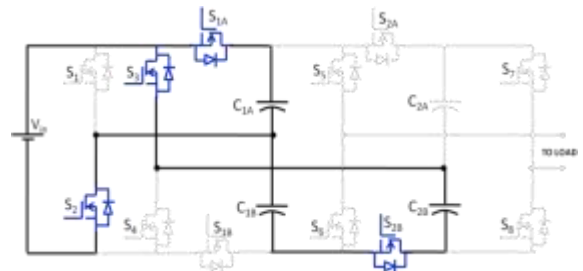


Fig 2 (a) Conduction Diagram for State A (b) Conduction Diagram for State B

There are five modes of operation of the proposed inverter to generated five levels. Operating modes of the proposed inverter are shown in figure 3 and explanations are given for each mode.

Mode 1: Figure 3(a) and figure 3(b) shows the mode 1 operation, in mode 1  $S_P$  group switches and  $S_5$  and  $S_7$  switches are in ON condition and the other switches are in OFF condition. Output voltage across the load is 0 volts since the input voltage is not connected to the load. Capacitor  $C_1$  and  $C_{2A}$  are in parallel to each other. Similarly when switches of  $S_N$  group and  $S_6$  and  $S_8$  are in ON condition a similar situation exists.

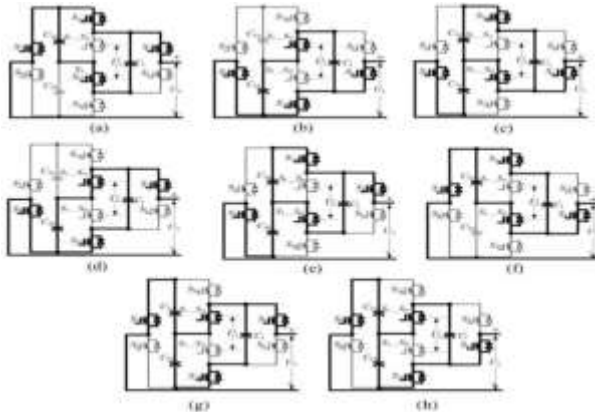


Fig 3. Modes of operation of the proposed inverter.

Mode 2: In Fig. 3(c) and 3(d), corresponds to mode 2, voltage value of  $2V_{in}$  can be obtained from the proposed converter. One operation state is that switches group  $S_P$ , switches  $S_6, S_8$  are turned ON and other switches are turned OFF, capacitors  $C_1$  and  $C_{2a}$  are in parallel connection, inverter has the output voltage of  $C_{2b}$ , as shown in Fig. 3(c). Fig. 3(d) shows another operation state with switches group  $S_N$ , switches  $S_5, S_8$  turned ON and other switches turned OFF, capacitors  $C_1$  and  $C_{2b}$  are in parallel connection, the inverter produces the voltage of  $C_{2b}$ .

Mode 3: In Fig. 3(e), corresponds to the mode 3 operation in this, switches group  $S_P$ , switches  $S_5, S_8$  become on-state, capacitors  $C_1$  and  $C_{2a}$  are parallel connection, the inverter outputs the summation voltage of capacitor  $C_{2a}$  and  $C_2$ .

Mode 4: In Fig. 3(f) and 3(g) corresponds to the mode 4 operation, switches group  $S_P$ , switches  $S_6, S_7$  are turned ON and capacitors  $C_1$  and  $C_{2a}$  are in parallel connection, the inverter outputs the reverse voltage of  $C_{2A}$  with value of  $-V_{in}$ . In Fig. 3(g), switches group  $S_N$ , switches  $S_5, S_7$  conduct and capacitors  $C_1$  and  $C_{2B}$  are in parallel connection, the inverter outputs the reverse voltage of  $C_{2A}$  with value of  $-2V_{in}$ .

Mode 5: In Fig. 3(h), corresponds to mode 5 operation, switch group  $S_N$ , switches  $S_6, S_7$  become on-state and capacitors  $C_1$  and  $C_{2B}$  are in parallel connection, the inverter produces the reverse voltage of  $C_{2A}$  and  $C_{2B}$  with value of  $-4V_{in}$ .

PERFORMANCE COMPARISON

The performance of the proposed inverter is compared in terms of active devices, diodes, capacitors, front end boost conversion, voltage stress, switching frequency, capacitor voltage balance control and number of DC sources with that of other similar type of inverters available in the literature. Table 1 shows a detailed comparison.

	Five Level Inverter			
	Diode Clamped	Capacitor Clamped	Cascaded H bridge	Proposed Inverter
Active Switches	8	8	8	12
Diodes	12	0	0	0
Capacit	4	10	2	4
Front End Boost Conversion	Needed	Needed	Needed	Not Needed
Voltage Stress	$0.25 U_B$	$0.25 U_B$	$0.5 U_B$	✓ $0.25 U_B$ (8 Nos) ✓ $0.5 U_B$ (2 Nos) ✓ $U_B$ (2 Nos)
Switching Frequency	$f_c$	$f_c$	$f_c$	$f_c$ (4 switches) $f_i$ (4 switches)
Capacitor Voltage Balance Control	Difficult [9]	Difficult [10]	Difficult	Easy
Number of DC sources	1	1	2	1

Table 1: Performance Comparison

### SWITCHING LOGIC

The switching logic of the proposed inverter is shown in figure 4. It has four level shifted carrier waveforms compared with the sinusoidal reference waveform.

From figure 4 it can be seen that four switches operates at low frequency which reduces the switching losses there by increasing the efficiency. Table 2 shows the switchinglogic of the proposed inverter in a simplified form.

Condition for Modulation and Carrier Wave		Switching States					
		S <sub>P</sub>	S <sub>N</sub>	S <sub>5</sub>	S <sub>6</sub>	S <sub>7</sub>	S <sub>8</sub>
U <sub>s</sub> >= U <sub>c</sub>	U <sub>s</sub> >= U <sub>A</sub>	1	0	1	0	0	1
	U <sub>s</sub> < U <sub>A</sub>	0	1	0	1	0	0
0 <= U <sub>s</sub> < U <sub>c</sub>	U <sub>s</sub> >= U <sub>B</sub>	1	0	0	1	0	1
	U <sub>s</sub> < U <sub>B</sub>	0	1	1	0	1	0
-U <sub>c</sub> <= U <sub>s</sub> < 0	U <sub>s</sub> >= U <sub>C</sub>	1	0	1	0	1	0
	U <sub>s</sub> < U <sub>C</sub>	0	1	0	1	0	1
U <sub>s</sub> < -U <sub>c</sub>	U <sub>s</sub> >= U <sub>D</sub>	1	0	0	1	1	0
	U <sub>s</sub> < U <sub>D</sub>	0	1	1	0	0	1

Table 2: Switching Logic of the proposed inverter.

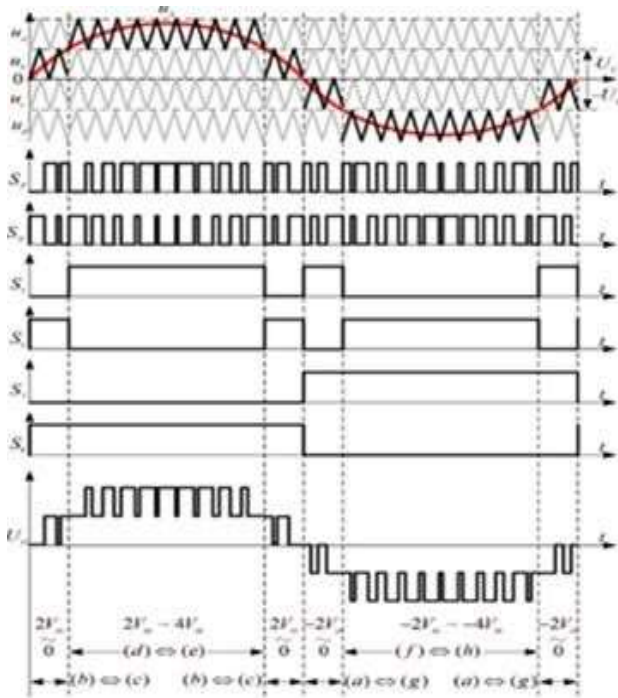


Figure 4 Switching logic of the proposed inverter.

### SIMULATION RESULTS

MATLAB/SIMULINK software is used to simulate the suggested inverter, and the results are shown in this section. According to figure 5, the suggested inverter is fed by dc voltage of 100 V and the voltage is increased to around 400 V peak. The current delivered to the load by the suggested inverter is close to 30 A peak, as illustrated in figure 6, making it suitable for high power applications. The switching patterns of the SP and SN switches are displayed in Figure 7. The switching patterns of the switches S5 and S6 are similarly shown in Figure 8. Figure 9 displays the switching patterns of switches S7 and S8.

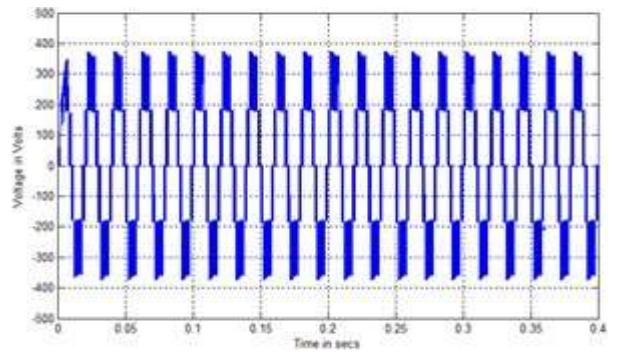


Fig 5. Load Voltage Waveform

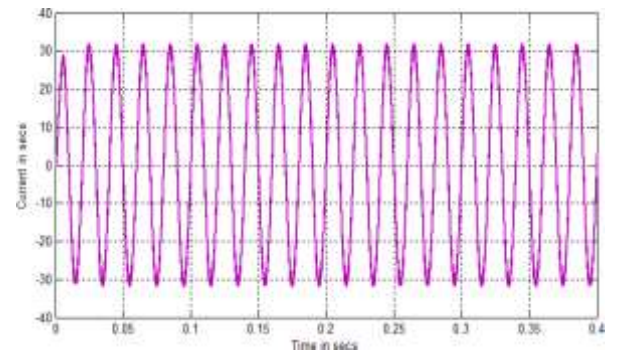


Fig 6. Load Current Waveform

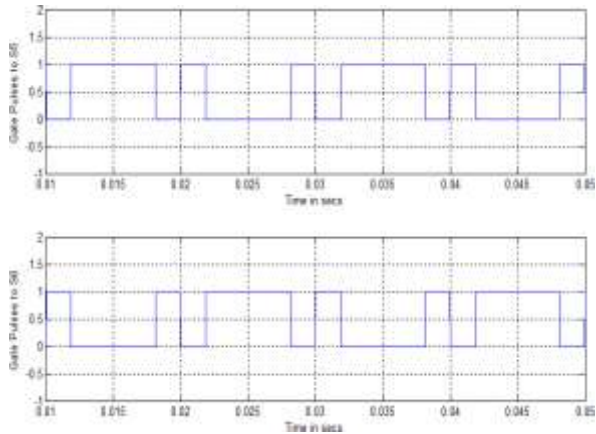


Fig 7 Switching pulses for  $S_P$  and  $S_N$  Switches.

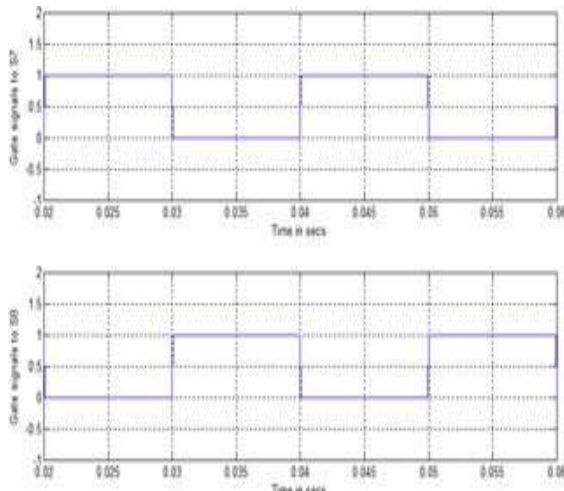


Fig 8 Switching pulses for  $S_5$  and  $S_6$  Switches.

Fig 9 Switching pulses for  $S_7$  and  $S_8$  Switches

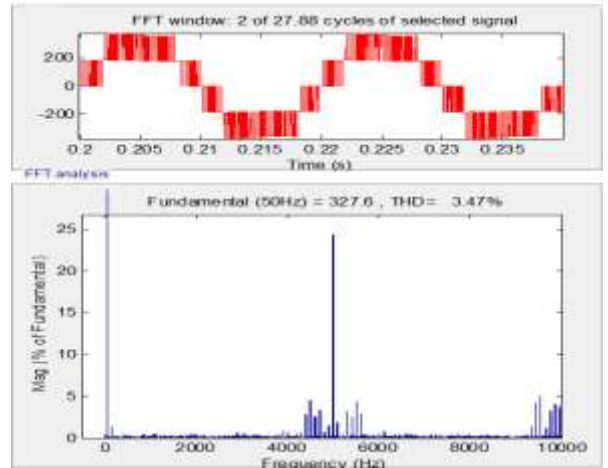
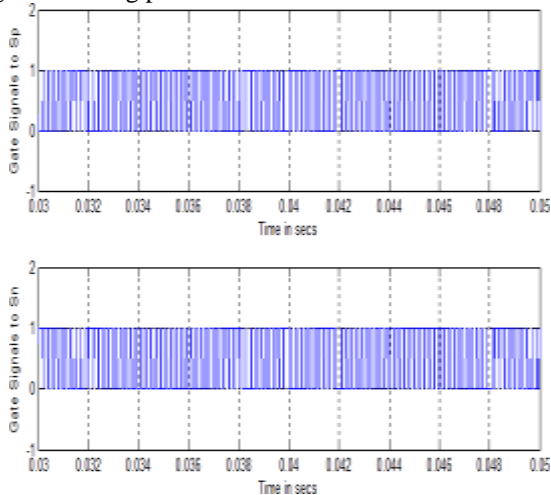


Fig 10 Output Voltage THD

Figure 10 displays the inverter's total harmonic distortion when it is working at full load. The proposed inverter's modulation index is adjusted from 0 to 1, and the inverter's performance is examined. It is discovered that when the modulation index is decreased, the number of levels drops to three. Figure 11 displays the voltage waveform with the lowered modulation index. The current waveform for a modulation index of 0.5 is shown in Figure 12. The total harmonic distortion is discovered to be less than 5%, which is the limit set by IEEE standards.

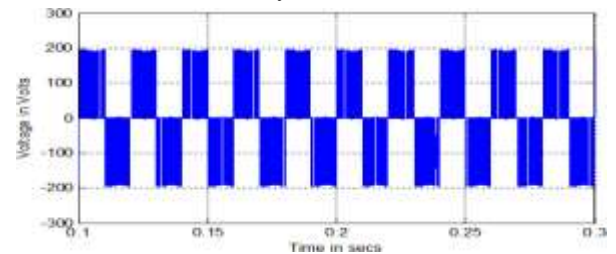


Fig 11 Load voltage with Modulation index = 0.5

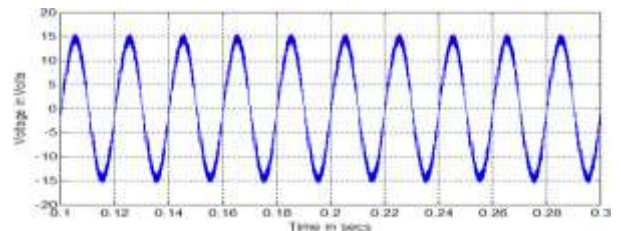


Fig 12 Load Current with Modulation index = 0.5

**CONCLUSION**

A brand-new single phase five level boost inverter that is appropriate for use with renewable energy sources is described. The suggested inverter's switches work at low frequency in some cases, which results in high

efficiency operation. When compared to other inverters suggested in the literature, the suggested inverter requires the fewest switching devices. Results from simulations are shown for various modulation indices.

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