International Journal of Computational Intelligence in Control

An Induction Motor Drive with Multilevel Inverter Fed and PWM Control Strategy

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ABSTRACT

Due to their numerous benefits, including lower common mode voltage, less voltage stress on power switches, and a lower dv/dt ratio to supply output voltage and current with lower harmonic contents, multilevel inverters have recently attracted a lot of attention in the application areas of medium voltage and high power. MLIs also offer the advantage that the harmonic components of line-to-line voltages fed to the load are reduced due to its switching frequency when compared to two-level inverter topologies at the same power ratings. Diode clamped MLI (DC-MLI), flying capacitor MLI (FC-MLI), and cascaded H-Bridge MLI are the three most used MLI topologies (CHB- MLI). According to the merging of current MLI topologies or using other techniques, the hybrid and asymmetric hybrid inverter topologies have been constructed.

IndexTerms--Multilevelinverters,dclinkvoltages,THD

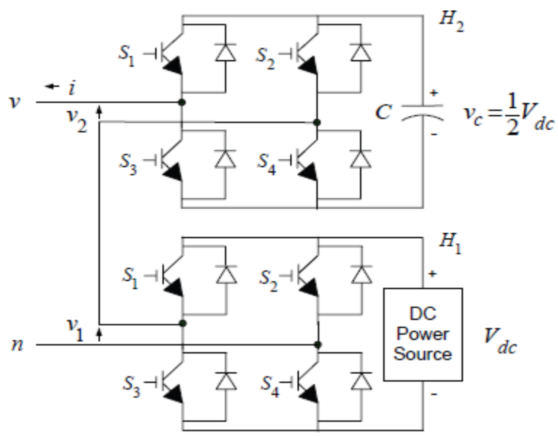
I. INTRODUCTION

Multilevel inverters are a novel class of power converter that has drawn the attention of power electronics engineers recently. The majority of multilevel inverters contain a setup of switches and voltage sources for capacitors. These switching devices can produce stepped output voltages with little harmonic distortion if they are properly controlled. Due to their ability to overcome obstacles, these multilevel inverters are commonly employed in industrial facilities and have gained public recognition as one of the emerging power converter fields. **The disadvantages of traditional inverters. Three unique topologies for multilevel inverters can be distinguished: diode clamped, flying capacitors, and cascaded H-bridge cells with independent DC sourcesa lot of topologies have also been proposed in recent years for multilevel converters that feature few switches and gate driver circuits. The key advantages of a multilayer inverter over a conventional two-level voltage inverter include a smaller output voltage step, lower harmonic components, improved electromagnetic compatibility, and lower switching losses. The usage of more semiconductors, complicated control circuitry, and the requirement for equilibrating the voltage at the boundaries of capacitors are the multilayer inverter's primary drawbacks.**

The switching frequency can be used to categories the modulation techniques employed in multilevel inverters. Classic carrier-based sinusoidal pulse width modulation (SPWM), which employs the phase-shifting technique to lessen the harmonics in the load voltage, is a very well-liked technique in industrial applications. In other techniques, the power semiconductor switches are often commutated once or twice throughout a cycle of the output voltages, producing a staircase waveform. These techniques typically operate at low switching frequencies. This family includes space vector control and multilayer selective harmonic elimination. Large numbers of electronic components, including programmable logic controllers and variable speed drives, are used in modern industrial processes. These industrial and commercial customers experience numerous issues with electricity quality.

II. MULTILEVELINVERTERS

In Figure 1, the basic layout of a cascaded multilayer inverter for a single phase system is depicted. A unique H-bridge circuit is associated with each individual voltage source (Vdc1, Vdc2, and Vdc3) and is used to connect them in cascade with other sources.Depending on the switching state of the switches in the circuit, each H-bridge circuit has four active switching elements that can provide an output voltage with either positive or negative polarity, or simply zero volts. Utilizing three voltage sources that are not equal, this multilayer inverter structureMagnitudes. It is fairly easy to generalize the numberof distinct levels. The S



number of sources or stagesandtheassociatednumberofoutputlevelcanbewrittenasfollows

Fig.1 Single-phase structure of a multilevel cascaded H-bridgesinverter

$$N_{level} = 2S + 1$$

For instance, the output wave form comprises seven levels if S=3, including 3Vdc, 2Vdc, 1Vdc, and 0. You can use the equation to determine the voltage on each level.

According to this architecture, there are exactly as many controlled switches as,

The multilayer inverter's output voltage is given as follows:

Sources of DC voltage A1, A2, and A3, respectively

Cascaded multilevel inverters' benefits include packaging and modularized design. This makes it possible to complete the manufacturing process faster and for less money. This topology's disadvantages include the high number of semiconductor switches and the requirement for a separate DC supply for each H-bridge.

ModifiedCascadedMultilevelInverter

Thegeneralstructureofaproposedcascadedmultilevel inverter is shown in Figure 3. This inverterconsists of a multi conversion cell and an H bridge. Amulticonversioncellconsistsofthreeseparatevoltagesources(Vdc1,Vdc2,and Vdc3),eachsourceconnected in cascade with other sources via a circuitconsistsofoneactiveswitchingelementandonediode that can make the output voltage source only inpositivepolaritywithseverallevels.OnlyOne H-Bridgeisconnectedwithmulticonversioncelltoacquirebothpositiveandnegativepolarity.Byturning on controlledswitches S1 (S2 andS3 turnoff) the output voltage +1Vdc (first level) is obtained.SimilarlyturningonofswitchesS1,S2(S3turnoff)

+2Vdc (second level) output is produced across theload.Similarly+3Vdclevelscanbeachievedbyturning on S1, S2, S3 switches as shown in Table I.The main advantage of proposed modified cascadedmultilevel inverter is seven levels with only use ofsevenswitches.TheSnumberofDCsourcesorstages and the associated number output level can becalculated byusingthe equationasfollows,

$$N_{level} = 2S + 1$$

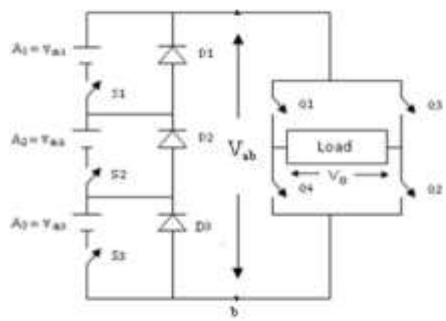


Fig.2Topologyformodifiedcascadedmultilevelinverter

For an example, if S=3, the output wave form willhavesevenlevels(±3Vdc,±2Vdc,±1Vdcand0).Similarly voltage on each stage can be calculated byusingthe equationasgiven,

$$A_i = 1V_{dc}(i = 1, 2, 3 \ldots)$$

The number switches usedin this topology is givenbythe equationasfollows,

$$N_{switch} = 2S + 4$$

Table-1BASICOPERATIONOFPROPOSEDMLI

S. No	Multiconversion Cell		H-Bridge		Voltage levels
	On switches	Off switches	On switches	Off switches	
1	S1, S2, S3	D1,D2,D3	Q1,Q2	Q3,Q4	$+3V_{dc}$
2	S1, S2, D3	S3, D1,D2	Q1,Q2	Q3,Q4	$+2V_{dc}$
3	S1, D2, D3	S2, S3, D1	Q1,Q2	Q3,Q4	$+1V_{dc}$
4	D1, D2, D3	S1, S2, S3	Q1,Q2	Q3,Q4	0
5	S1, D2, D3	S2, S3, D1	Q3,Q4	Q1,Q2	$-1V_{dc}$
6	S1, S2, D3	S3, D1,D2	Q3,Q4	Q1,Q2	$-2V_{dc}$
7	S1, S2, S3	D1,D2,D3	Q3,Q4	Q1,Q2	$-3V_{dc}$

Table I displays the switching table for the redesigned cascaded multilevel inverter. It shows that among the paralleled switches, there is only one switch that is ON for each voltage level. The H-bridge inverter outputs a stepped or roughly sinusoidal AC waveform from the stepped DC voltage that the multi conversion cell has converted into. Switches Q1 and Q2 will be switched on in this H-bridge for the positive half cycle, while Q3 and Q4 must be turned on for the negative half cycle. The topology for the modified cascaded multilevel inverter is shown in Figure 2.SevenlevelCHBInverter

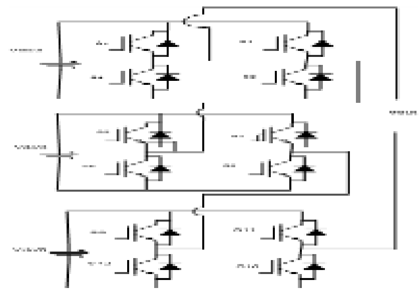


Fig.3 Shows the seven level multilevel inverter and Table shows theswitchingstatesofthesevenlevelinverter

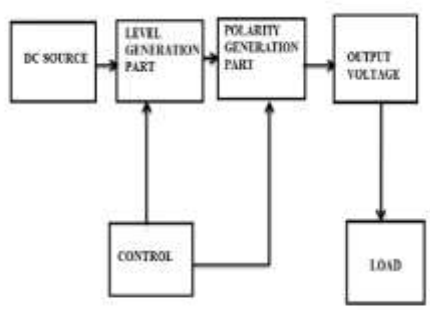
TABLE-2FULLH-BRIDGEOFSEVENLEVEL INVERTER

Switches Turn ON	Voltage Level
S1,S2,S6,S8,S10,S12	Vdc/3
S1,S2,S5,S6,S10,S12	2Vdc/3
S1,S2,S5,S6,S9,S10	Vdc
S2,S4,S6,S8,S10,S12	0
S3,S4,S6,S8 S10,S12	-Vdc/3
S3,S4,S7,S8,S10,S12	-2Vdc/3
S3,S4,S7,S8,S11,S12	-Vdc

A. SUGGESTIVE NEW MULTILEVEL TOPOLOGY

GeneralDescription

Traditionally used cascaded multilevel inverters need a lot of switches, and the power switches are coupled to produce an output with both positive and negative polarities. The proposed multilevel inverter does not need the use of all switches at high frequency. In this design, the level and polarity generation components of the output voltage are separated. Positively polarized levels are produced by the level generating component.Andthepolarity generation part generates the polarity ofthe output voltage. Level generation



part needshigh frequency switches and polarity generationpart requires low-frequency switches operating atlinefrequency.Fig.1showsthegeneralblockdiagramofreversevoltage topology.

Fig.4.Generalblockdiagram

With this design, three phase applications are possible and fewer switches are needed. For SPWM, only half as many conventional carriers are required. In the proposed system, only five carriers are required, compared to the 10 required for SPWM for eleven-level conventional converters. Positive voltage is given to the polarity production component in order to generate polarity. The key benefit is that there are fewer carriers required for multilevel inverter control. For this structure, distinct DC sources are required. Compared to traditional multilayer inverters, the suggested multilevel inverter is more efficient. According to Fig. 5, an eleven inverter needs fourteen switches and five DC sources.In Fig. 5, the right side of the circuit generates the polarity of the output voltage, while the left side of the circuit generates the necessary output levels. When the voltage polarity needs to be altered to a negative one, the circuit's right-hand section, known as the polarity generation part, reverses the level generation part's output.

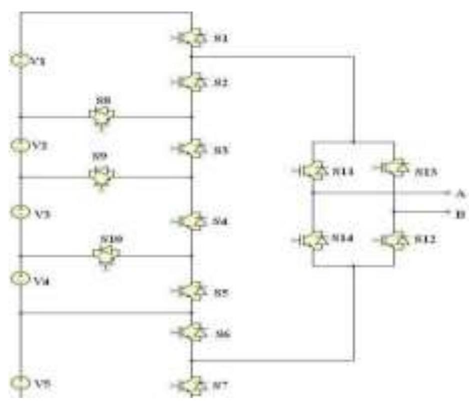


Fig.5 Schematic of a eleven-level inverter in single phase

By duplicating the middle stage as depicted in Fig. 5, this topology can readily be expanded to greater voltage levels. As a result, this design is modular and is easily expandable to higher voltage levels by including the intermediate stage in Fig. 5. The same theory applies to three-phase applications as well. This architecture makes use of segregated DC supply. As a result of the set dc voltage values, it does not have voltage balancing issues. It uses only a third of the isolated power supplies needed by a cascade-type inverter in contrast. This topology's switching sequence is flexible and redundant. ModesofOperation

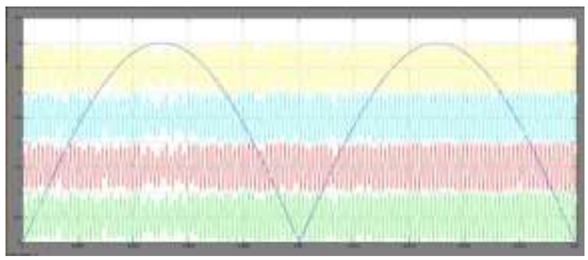
For the purpose of minimising the undesirable voltage levels, the switching modes are chosen such that the switching transitions become minimum. By doing this, switching power loss will be reduced. For levels 0 through 5, the switches (2-3-4-5-6), (2-3-4-5-7), (2-3-4-10-7), (2-7-8) and (1-7) are utilized, accordingly. The total of the voltage sources is the output voltage TableIshowstheswitching sequences.

TABLE3

Lev el /Mo de	0	1	2	3	4	5
1	2,3, 4,5, 6	2,3, 4,5, 7	2,3,4, 10,7	2,3,9 ,7	2,8, 7	1, 7
2		1,8, 3,4, 5,6	*1,9,4,5 ,6*	1,10, 5,6	1,6	

B. ControlStrategies

A carrier waveform VC and a modulating signal VA are compared in the carrier based PWM approach to satisfy switching states. The triangle signal VC is at frequency FC and amplitude VC, whereas the modulating signal VA is a sinusoidal at frequency FC and amplitude VA. The low frequency polarity generation component drive signals are created with line frequency (50Hz) in this case and only change at zero-voltage crossings. SPWM is



employed to drive the high frequency switches. In the suggested topology, an n-level inverter's a-phase modulation signal is compared to the (n-1)/2 triangle waveforms utilized in typical cascaded multilevel inverters. Figure 6 depicts the modular and four carriers.

Fig6.Modulatorand SPWMcarrier

C. Numberofcomponents

The quantity of the system's components is indirectly inversely related to its reliability. This architecture has the major benefit of requiring fewer high-switching frequency components. The converter becomes more dependable as the number of high-frequency switches decreases. As a result, this topology's reliability is significantly enhanced. Additionally, expensive and prone to damage are high frequency switches and diodes. An N level conventional cascaded H bridge multilevel inverter, where N is the number of the output voltage level, requires 2(N-1) switching devices. For a N level inverter in this topology, only ((N-1) +4) switches are required. This architecture has fewer switches than others, and as voltage levels rise, fewer switches will be present. The full bridge converter's switches operate at line frequency.Requiredcomponentsfordifferenttopologiesare giveninTable 4.

Inverter type	NPC	Flying capacitor	Cascade	RV
Main switches	6(N-1)	6(N-1)	6(N-1)	3((N-1)+4)
main diodes	6(N-1)	6(N-1)	6(N-1)	3((N-1)+4)
Clamping diodes	3(N-1)(N-2)	0	0	0
DC bus capacitors/ Isolated supplies	(N-1)	(N-1)	3(N-1)/2	(N-1)/2
Flying capacitors	0	$\frac{3}{2}$(N-1)(N-2)	0	0
Total numbers	(N-1)(3N+7)	$\frac{1}{2}$(N-1)(3N+20)	$\frac{27}{2}$(N-1)	(13N+35)/2

Table4

III. MATLAB/SIMULINKRESULTS

Here the simulation is carried by two different casesproposedsevenlevelinverterandelevenlevelinverter topology

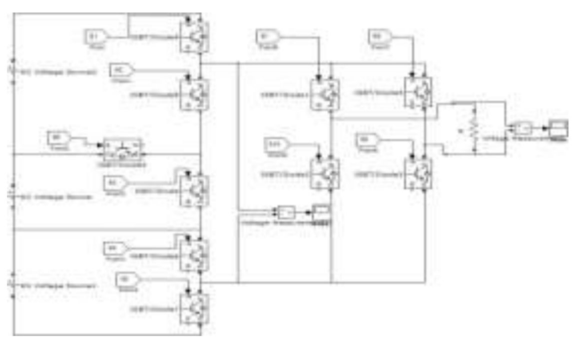


Fig.7showstheSimulationCircuitdiagramSinglephaseSevenLevel Inverter

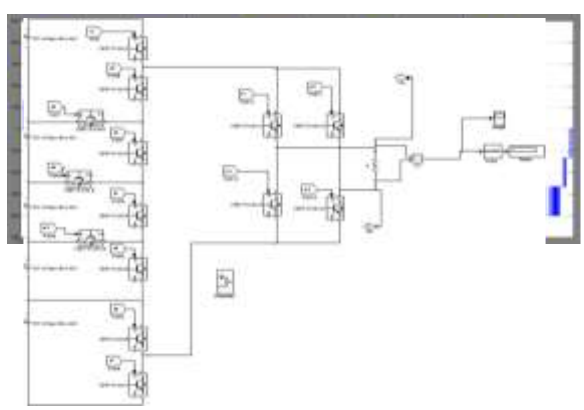


Fig.8 Simulation output voltage waveforms forseven -levelInverter

Fig.9showstheSimulationCircuitdiagramSinglephaseelevenLevel Inverter

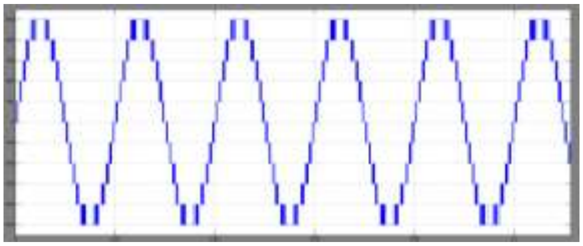


Fig.10 Simulation output voltage waveforms for eleven-levelInverter

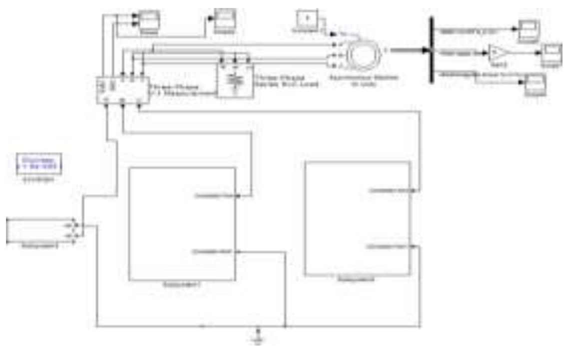


Fig.11 Three-phase Inverter feeding Induction Motor Drive for 7-level

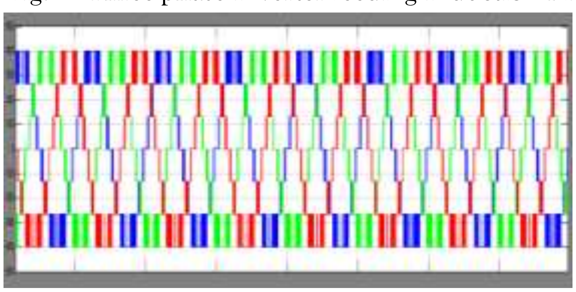


Fig.12ThreePhaseoutputwaveformfor7-level

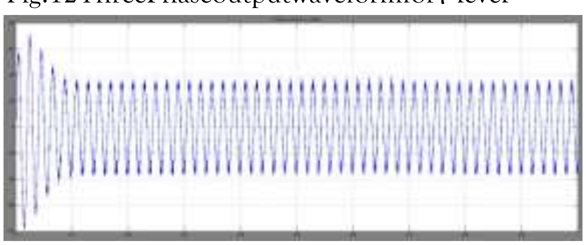


Fig.13StatorcurrentsoftheMotor for7-level

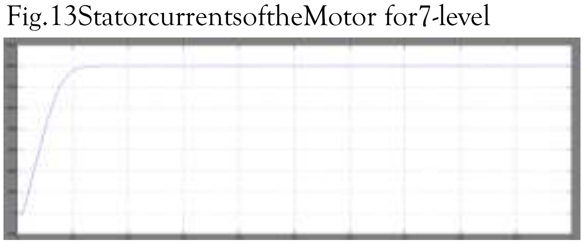
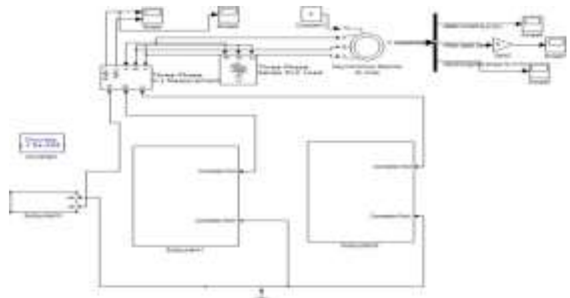


Fig.14SpeedcharacteristicsoftheInductionMotor for7-level



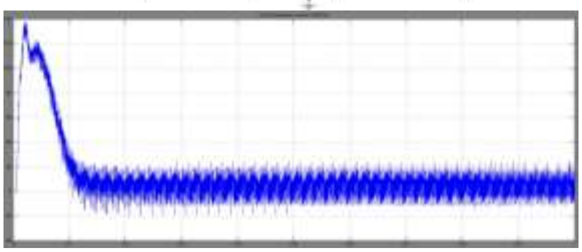


Fig.15TorqueresponseoftheMotorfor7-level

Fig.16 Three-phase Inverter feeding Induction Motor Drive for 11-level

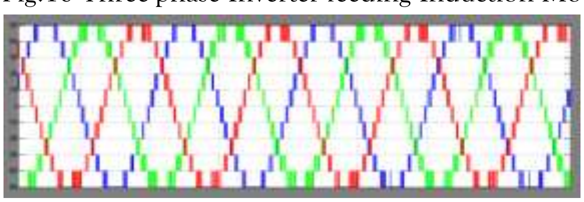


Fig.17ThreePhaseoutputwaveformfor11-level

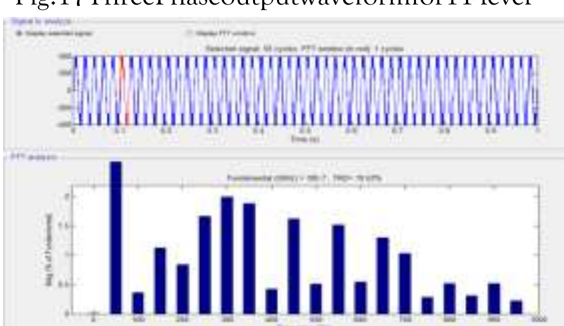


Fig.18HarmonicAnalysisof7-levelinverteris19.52%

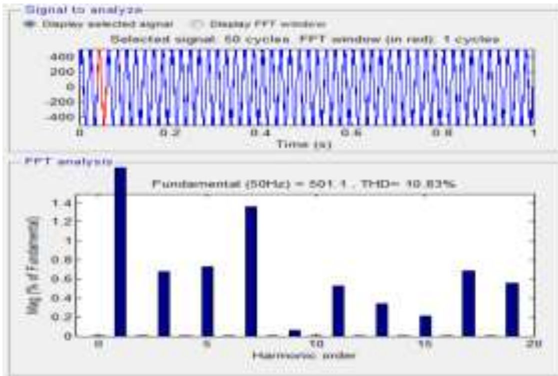


Fig.19HarmonicAnalysisof11-levelinverteris10.83%

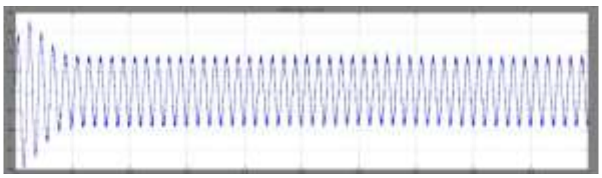


Fig.20StatorcurrentsoftheMotorfor11-level

Fig.21SpeedcharacteristicsoftheInductionMotorfor11-level

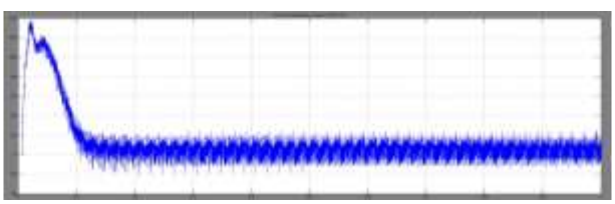


Fig.22TorqueresponseoftheMotorfor11-level

The output waveforms of the simulated proposed inverter demonstrate the inverter's effectiveness. The results of the speed, torque, and stator characteristics of the induction motor are also shown when this inverter is linked to the induction motor drive. To operate the inverter, level-shifted sinusoidal pulse width modulation is used, which employs a remarkably low amount of carrier waves. By making the necessary adjustments to the circuit design, the proposed topology can be expanded to any number of layers. One thing to keep in mind is that multilevel converters are no longer useful when taking into account the upper levels.

A new eleven-level inverter layout with fewer power electronics switches is presented in this research. Future upgrades to this new breed of multi-level inverter will allow for output at any level. Numerous industrial applications, including HVDC, FACTS, EV, PV systems, UPS, and industrial drive applications, have utilised multilevel inverters. Switching operations in the suggested topology are divided into high- and low-frequency components. For all of these applications, the suggested topology is more practical than cascaded inverter topology because it has a less complicated control technique, lower associated costs, and lower THD. This uses the carrier-based PWM technique with the SPWM tactic. Since the SPWM control method only employs positive carriers for PWM control, it is less complicated.

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